REMARKS

Claims 1-15 remain in this application. Claims 1, 6, 11 and 12 have been amended. Figure 5 has been amended to correct a typographical error.

Claims 1-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kochi et al. in view of Yoshida et al. Applicant respectfully traverses this rejection with respect to claims 1-10 and 13-15, because the cited references, alone or in combination, do not disclose or suggest features of the outputting units or outputting step of the present invention as described in independent claims 1 and 6.

More specifically, claim 1 describes a plurality of outputting units, each for receiving a result of the operation of a corresponding one of operating units and outputting the result of the operation for each of the corresponding one of a plurality of elements that are disposed in a matrix of an optical area (see Fig. 4). Claim 6 also describes this feature in a method format.

The Kochi et al. reference discloses in an embodiment shown in Figs. 19A and 19B (which is cited in the Office Action as the basis for the rejection), an arithmetic operation output 50 provided in a chip arrangement for performing high-speed image processing. The chip arrangement also includes an image data sensing unit 60 having rows and columns of light-receiving portions or pixels 41. As clearly shown in 19A, the chip arrangement of Kochi et al. uses a single output (i.e., the one output shown in Fig. 19A for outputting the results of a single arithmetic operation output unit 54) for all the numerous pixels of the sensing unit. The Kochi et al. reference does not disclose or suggest the plurality of outputting units corresponding to the plurality of operating units of the present invention.

The Yoshida et al. reference is cited for teaching "a plurality of arithmetic units for parallel processing." Even if this is correct, this reference, however, still does not disclose or suggest a plurality of outputting units corresponding to the operating units, each of which operates a signal obtained for corresponding one of the elements disposed in a matrix, as in the present invention. Therefore, even if the teachings of Kochi et al. were combined with Yoshida et al., the resulting device still would not disclose or suggest the plurality of outputting units, each for receiving a result of the operation of a corresponding one of the operating units and outputting the result of the operation for each of the corresponding one of the elements of the

present invention. For these reasons, claims 1 and 6, and their dependent claims 2-5, 7-10 and 13-15 are allowable over the cited references.

Applicant respectfully traverses with respect to claims 11 and 12 because the cited references, alone or in combination, do not disclose or suggest the features of the present invention in which the operation of the operating means includes a plurality of modes which are represented by different expressions from each other, as described in claims 11 and 12. With respect to the arithmetic operation output unit 50, the Kochi et al. reference merely states that "this arrangement performs arithmetic operations on the basis of analog signals output from the sensor. However, when the A/D converter of the present invention is arranged between each memory and the output bus line, a digital correlation arithmetic operation can be realized, needless to say." This is the extent of any disclosure regarding arithmetic operations in Kochi et al. The Kochi et al. reference, therefore, does not disclose or suggest the plurality of modes that are represented by different expressions from one another, as described in claims 11 and 12. Similarly, the Yoshida et al. reference is also silent as to the different expressions describing the plurality of modes. Therefore, even if these references were combined, the resulting device still would not use the different plurality of modes described in claims 11 and 12. For these reasons, claims 11 and 12 are also allowable over the cited references.

In light of the above, Applicants respectfully submit that claims 1-15 are now in condition for allowance, which is respectfully requested.

Respectfully submitted,

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